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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-----------------|-------------|----------------------|---------------------|------------------|
|-----------------|-------------|----------------------|---------------------|------------------|

10/849,749

05/19/2004

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04/14/2009

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EXAMINER

SAVLA, ARPAN P

ART UNIT

PAPER NUMBER

2185

MAIL DATE

DELIVERY MODE

04/14/2009

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

DETAILED ACTION

Response to Amendment

This Office action is in response to Applicant's communication filed December 29, 2008 in response to the Office action dated July 29, 2008. Claims 2, 3, 5, 6, 8, 10, 12, 13, 16, 18, 20-22, 25, and 26 have been amended. New claims 30-35 have been added. Claims 2-6, 8-13, 16, 18, 20-22, and 25-35 are pending in this application.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. **Claims 2-4, 6, 12, 18, and 22** are rejected under 35 U.S.C. 102(b) as being anticipated by Don Pannell, "Clause 22 Access to Clause 45 Registers" (hereinafter "Pannell").

3. **As per claim 30**, Pannell discloses a method for expanding addressing capability of a plurality of registers and connected to an interface comprising:

designating at least two of the plurality of registers as a block of registers (pg. 14, the "65,536 Registers"); *It should be noted that the 65,536 registers comprise at least one "block of registers"*

providing a plurality of such blocks of registers (pg. 14, the "65,536 Registers");

designating a first register within the plurality of registers that is separate from the blocks of registers **for** selectively characterizing at least one of such blocks of registers as an indicated block of registers such that any of the registers of the indicated block of registers may be addressed without adjusting a pointer, the first register being compatible with IEEE standard 802.3 clause 22 and designated by the standard as available for vendor specification (pg. 14, the “Addr Reg”; pg. 10, the “Management Frame Fields - Clause 45” table); *It should be noted that the term “for” renders the limitation reciting “selectively characterizing...” as merely a recitation of intended use of the claimed first register. It should also be noted that the “Addr Reg” is analogous to the “first register.” Lastly, it should be noted that the Addr Reg is used to address (i.e. characterize) the block of 65,536 Registers.*

and designating a second register within the plurality of registers that is separate from the blocks of registers **for** specifying at least one operation for the indicated block of registers, the second register being compatible with IEEE standard 802.3 clause 22 and designated by the standard as available for vendor specification (pg. 14, the “C45 R/W Control”; pg. 10, the “Management Frame Fields - Clause 45” table). *It should be noted that the term “for” renders the limitation reciting “specifying...” as merely a recitation of intended use of the claimed second register. It should also be noted that the “C45 R/W Control” is analogous to the “second register.” Lastly, it should be noted that the “opcode” stored in C45 R/W Control specifies at least one operation for the block of 65,536 Registers.*

4. **As per claim 31**, Pannell discloses a system for expanding the addressing capability of a plurality of registers, the system comprising:

a plurality of blocks of registers, each block of registers having at least two registers (pg. 14, the “65,536 Registers”);

a location register separate from the plurality of blocks of registers **for** selectively characterizing at least one of the blocks of registers as a specified block of registers such that any of the registers of the indicated block of registers may be addressed without adjusting a pointer, the location register being compatible with IEEE standard 802.3 clause 22 and designated by the standard as available for vendor specification (pg. 14, the “Addr Reg”; pg. 10, the “Management Frame Fields - Clause 45” table); *It should be noted that the term “for” renders the limitation reciting “selectively characterizing...” as merely a recitation of intended use of the claimed location register. It should also be noted that the “Addr Reg” is analogous to the “location register.”*

a control register separate from the plurality of blocks of registers **for** selecting at least one operational code for the specified block of registers and specifying at least one port number for the specified block of registers, the control register being compatible with IEEE standard 802.3 clause 22 and designated by the standard as available for vendor specification (pg. 14, the “C45 R/W Control”; pg. 10, the “Management Frame Fields - Clause 45” table); *It should be noted that the term “for” renders the limitation reciting “selecting...and specifying...” as merely a recitation of intended use of the claimed control register. It should also be noted that the “C45 R/W Control” is analogous to the “control register.”*

and a control engine **operable to** access the operational code for the specified block of registers and act on the specified block of registers at each of the specified port numbers in accordance with the operational code (pg. 14, the “Existing Clause 22 STA”). *It should be noted that the term “operable to” renders the limitation reciting “access...and act...” as merely a recitation of intended use of the claimed location register. It should also be noted that the “Existing Clause 22 STA” is analogous to the “control engine.” It should be noted that the STA (station management) accesses and controls the PHY (physical layer interface). Thus, it is inherently required the STA access and control the block of 65,536 Registers within the PHY in accordance with the Opcode signal.*

5. **As per claim 2**, Pannell discloses the first register includes a block selector **for** selectively characterizing at least one of such blocks of registers as an indicated block of registers (pg. 14, the “Device Select” signal). *It should be noted that the Device Select signal sent to the C45 R/W Control and then eventually to the Addr Reg effectively acts as a “block selector” for the Addr Reg.*

6. **As per claim 3**, Pannell discloses the second register includes an operational code (pg. 14, the “the Opcode” being sent to the C45 R/W Control). *It should be noted that “Opcode” is analogous to “operational code.”*

7. **As per claim 4**, Pannell discloses the second register includes a port indicator (pg. 14, the “Port Select” signal). *It should be noted that the Port Select signal sent to the MUX, then AND gate, and eventually to the C45 R/W Control effectively acts as a “port indicator” for the C45 R/W Control.*

8. **As per claim 6**, Pannell discloses said location and control registers comprise registers compatible with IEEE standard 802.3 clause 22 (pg. 25).
9. **As per claim 12**, Pannell discloses said location register includes a block selector indicating said block. (pg. 14, the “Device Select” signal). *See the citation note for claim 2 above.*
10. **As per claim 18**, Pannell discloses said control register is **operable to** specify a plurality of ports (pg. 7, line 5; pg. 14, the “5 Port Address Pins” and the “Port Select” signal).
11. **As per claim 22**, Pannell discloses said location and control registers are registers specified by IEEE standard 802.3 clause 22 (pg. 25).
12. **As per claim 33**, Pannell discloses said control register is **operable to** store an operational code (pg. 14, the “the Opcode” being sent to the C45 R/W Control).
13. **As per claim 16**, Pannell discloses said control register is further **operable to** store a register indicator indicative of a register within said block (pg. 14, the signal sent from the “C45 R/W Control” to the “Addr Reg”). *It should be noted that the Addr Reg gets all its information from the C45 R/W Control, therefore, because the Addr Reg addresses the block of 65,536 Registers, it is inherently required the C45 R/W Control stores register addresses (i.e. register indicators) of registers within the block of 65,536 Registers.*
14. **As per claim 34**, Pannell discloses said control register is further **operable to** store a port indicator (pg. 14, the “Port Select” signal).

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

16. **Claims 5, 13, 20, 26-29, 32, and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Don Pannell, "Clause 22 Access to Clause 45 Registers" (hereinafter "Pannell") in view of Law et al., "IEEE P802.3ae 10Gb/s Ethernet MDC/MDIO Proposal" (hereinafter "Law") and Nick Parlante, "Pointers and Memory" (hereinafter "Parlante").**

17. **As per claim 26**, Pannell discloses a method for expanding addressing capability of a plurality of registers, comprising:

designating at least two of the plurality of registers as a block of registers (pg. 14, the "65,536 Registers");

providing a plurality of such blocks of registers (pg. 14, the "65,536 Registers");

designating a first register within the plurality of registers that is separate from the blocks of registers **for** selectively characterizing at least one of such blocks of registers as an indicated block of registers, such that any of the registers of the indicated block of registers may be addressed without adjusting a pointer, the first register being compatible with IEEE standard 802.3 clause 22 and designated by the standard as available for vendor specification (pg. 14, the "Addr Reg"; pg. 10, the "Management

Frame Fields - Clause 45" table); *It should be noted that the term "for" renders the limitation reciting "selectively characterizing..." as merely a recitation of intended use of the claimed first register.*

designating a second register within the plurality of registers that is separate from the blocks of registers **for** specifying at least one operation for the indicated block of registers, the second register being compatible with IEEE standard 802.3 clause 22 and designated by the standard as available for vendor specification (pg. 14, the "C45 R/W Control"; pg. 10, the "Management Frame Fields - Clause 45" table). *It should be noted that the term "for" renders the limitation reciting "specifying..." as merely a recitation of intended use of the claimed second register.*

Pannell does not disclose the first register including a pointer to a plurality of location registers that each indicates at least one of the blocks of registers;

the second register including a pointer to a plurality of control registers in which each control register includes an operational code;

and associating said plurality of location registers with said plurality of control registers such that a first operational code is associated with a first of such blocks of registers and a second operation code is associated with a second of such blocks of registers.

Law discloses each location register indicates at least one of the blocks of registers (Slide 5, registers 2 and 3);

and each control register includes an operational code (Slide 5, registers 0 and 9; Slide 9, "OP");

and associating said plurality of location registers with said plurality of control registers such that a first operational code is associated with a first of such blocks of registers and a second operation code is associated with a second of such blocks of registers (Slide 9, "OP"). *It should be noted that the control registers are associated with the location registers and that all control registers contain "opcode" (i.e. "OP").*

Pannell and Law are analogous art because they are from the same field of endeavor, that being IEEE 802.3 systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine Law's MDC/MDIO proposal and Pannell's Clause22/Clause45 proposal because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of providing indirect address register access so as to expand the number of registers that can be used.

The combination of Pannell/Law does not disclose the first register including a pointer to a plurality of location registers;

and the second register including a pointer to a plurality of control registers.

Parlante discloses pointers (pg. 3, 1st paragraph).

The combination of Pannell/Law and Parlante are analogous art because they are from the same field of endeavor, that being memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Parlante's pointers within Pannell/Law's 802.3 system.

The motivation for doing so would have been because pointers allow different sections of code to share information easily. You can get the same effect by copying information back and forth, but pointers solve the problem better. Also, pointers enable complex "linked" data structures like linked lists and binary trees (Parlante, pg. 3, 2nd paragraph).

18. **As per claim 27**, the combination of Pannell/Law/Parlante discloses the first register includes a block selector **for** selectively characterizing at least one of such blocks of registers as an indicated block of registers (Pannell, pg. 14, the "Device Select" signal). *See the citation note for claim 2 above.*

19. **As per claim 28**, the combination of Pannell/Law/Parlante discloses the second register includes a port indicator (Pannell, pg. 14, the "Port Select" signal). *See the citation note for claim 4 above.*

20. **As per claim 29**, the combination of Pannell/Law/Parlante discloses said location and control registers comprise registers compatible with IEEE standard 802.3 clause 22 (Pannell, pg. 25).

21. **As per claim 5**, Pannell does not disclose wherein said first register comprises a pointer to a plurality of location registers, each of the plurality of location registers indicating at least one such block of registers;

wherein said second register comprises a pointer to a plurality of control registers, each of the plurality of control registers comprising an operational code;

and wherein said plurality of location registers are associated with said plurality of control registers such that a first operational code is associated with a first of such

blocks of registers and a second operational code is associated with a second of such blocks of registers.

Law discloses each of the plurality of location registers indicating at least one such block of registers (Slide 5, registers 2 and 3);

each of the plurality of control registers comprising an operational code (Slide 5, registers 0 and 9; Slide 9, "OP");

and wherein said plurality of location registers are associated with said plurality of control registers such that a first operational code is associated with a first of such blocks of registers and a second operational code is associated with a second of such blocks of registers (Slide 9, "OP"). *It should be noted that the control registers are associated with the location registers and that all control registers contain "opcode" (i.e. "OP").*

Pannell and Law are analogous art because they are from the same field of endeavor, that being IEEE 802.3 systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine Law's MDC/MDIO proposal and Pannell's Clause22/Clause45 proposal because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of providing indirect address register access so as to expand the number of registers that can be used.

The combination of Pannell/Law does not disclose wherein said first register comprises a pointer to a plurality of location registers,

wherein said second register comprises a pointer to a plurality of control registers.

Parlante discloses pointers (pg. 3, 1st paragraph).

The combination of Pannell/Law and Parlante are analogous art because they are from the same field of endeavor, that being memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Parlante's pointers within Pannell/Law's 802.3 system.

The motivation for doing so would have been because pointers allow different sections of code to share information easily. You can get the same effect by copying information back and forth, but pointers solve the problem better. Also, pointers enable complex "linked" data structures like linked lists and binary trees (Parlante, pg. 3, 2nd paragraph).

22. **As per claim 13**, the combination of Pannell/Law/Parlante discloses said location register includes a pointer to a block selector (Pannell, pg. 14, the "Device Select signal"; Law, Slide 5, registers 2 and 3; Parlante, pg. 3, 1st paragraph).

23. **As per claim 20**, Pannell does not disclose wherein said location register includes a pointer to a plurality of location registers, each indicating a register block;

and wherein said control register includes a pointer to a plurality of control registers, each of the plurality of control registers storing a respective operational code, and wherein said plurality of locations registers are associated with said plurality of

control registers such that a first operational code is associated with a first block and a second operational code is associated with a block.

Law discloses said location register indicates a register block (Slide 5, registers 2 and 3);

and each of the plurality of control registers storing a respective operational code (Slide 5, registers 0 and 9; Slide 9, "OP"), and wherein said plurality of locations registers are associated with said plurality of control registers such that a first operational code is associated with a first block and a second operational code is associated with a block (Slide 9, "OP"). *See the citation note for the similar limitation in claim 5 above.*

Pannell and Law are analogous art because they are from the same field of endeavor, that being IEEE 802.3 systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine Law's MDC/MDIO proposal and Pannell's Clause22/Clause45 proposal because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of providing indirect address register access so as to expand the number of registers that can be used.

The combination of Pannell/Law does not disclose wherein said location register includes a pointer to a plurality of location registers;

and wherein said control register includes a pointer to a plurality of control registers.

Parlante discloses pointers (pg. 3, 1st paragraph).

The combination of Pannell/Law and Parlante are analogous art because they are from the same field of endeavor, that being memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Parlante's pointers within Pannell/Law's 802.3 system.

The motivation for doing so would have been because pointers allow different sections of code to share information easily. You can get the same effect by copying information back and forth, but pointers solve the problem better. Also, pointers enable complex "linked" data structures like linked lists and binary trees (Parlante, pg. 3, 2nd paragraph).

24. **As per claim 32**, the combination of Pannell/Law/Parlante discloses said location register includes a pointer to a plurality of location registers, each of the plurality of location registers including a block selector (Pannell, pg. 14, the "Addr Reg"; pg. 10, the "Management Frame Fields - Clause 45" table, the "Device Select signal"; Law, Slide 5, registers 2 and 3; Parlante, pg. 3, 1st paragraph).

25. **As per claim 35**, the combination of Pannell/Law/Parlante discloses said control register includes a pointer to a plurality of control registers, each having an operational code (Pannell, pg. 14, the "C45 R/W Control"; pg. 10, the "Management Frame Fields - Clause 45" table; Law, Slide 5, registers 2 and 3; Parlante, pg. 3, 1st paragraph).

26. Claims 8-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pannell in view of Law.

27. **As per claim 8**, Pannell discloses all the limitations of claim 8 except the operational code specifies an operation to be performed on the specified block of registers.

Law discloses the operational code specifies an operation to be performed on the specified block of registers (Slide 9, “OP” and “Access Type” table).

Pannell and Law are analogous art because they are from the same field of endeavor, that being IEEE 802.3 systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine Law’s MDC/MDIO proposal and Pannell’s Clause22/Clause45 proposal because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of providing indirect address register access so as to expand the number of registers that can be used.

28. **As per claim 9**, the combination of Pannell/Law discloses the operation is restricting the specified block of registers to read operations only (Law, Slide 9, OP “10, Read”).

29. **As per claim 10**, the combination of Pannell/Law discloses the operational code specifies control sequencing information (Law, Slide 9, OP “11, Post Read Inc Address”).

30. **As per claim 11**, the combination of Pannell/Law discloses the control sequencing information instructs the control engine to proceed to a next block after completing operations with the specified block (Law, Slide 9, OP “11, Post Read Inc Address”).

31. **Claim 21 is rejected under 35 U.S.C. 103(a) as being obvious over Pannell in view of Tsushima et al. (U.S. Patent 5,872,989) (hereinafter “Tsushima”).**

32. **As per claim 21**, Pannell discloses all the limitations of claim 21 except said operational code each encode an operation selected from the group of operations consisting of pointer handling and stream looping.

Tsushima discloses said operational code each encode an operation selected from the group of operations consisting of pointer handling and stream looping (col. 6, lines 9-23; col. 7, lines 22-34; Fig. 9; Fig. 11).

Pannell and Tsushima are analogous art because they are from the same field of endeavor, that being memory systems using registers.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to apply Tsushmia’s read and write pointers (known technique) to Pannell’s 802.3 system (a known system) ready for improvement to yield the predictable results of handling a large capacity physical register file even if the register specifying field in the instruction is small.

33. **Claim 25 is rejected under 35 U.S.C. 103(a) as being obvious over Pannell in view of Webb et al. (U.S. Patent 5,694,587) (hereinafter “Webb”).**

Pannell discloses a location register (pg. 14, the “Addr Reg”).

Pannell does not disclose a mask register following the location register and specifying a mask for the specified block of registers.

Webb discloses a mask register specifying a mask (col. 6, line 67 – col. 7, line 3; col. 7, lines 40-42).

Pannell and Webb are analogous art because they are from the same field of endeavor, that being computer systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Webb's mask register within Pannell's 802.3 system.

The motivation for doing so would have been to allow fast access to mask (Webb, col. 7, line 41).

Response to Arguments

34. Applicant's arguments filed December 29, 2008 with respect to **claims 2-6, 8-13, 16, 18, 20-22, and 25-35** have been fully considered but they are not persuasive.

35. With respect to Applicant's argument regarding the first register of claim 26, which appears on pages 9-10 of the communication filed December 29, 2008, the Examiner respectfully disagrees. Firstly, when taking the broadest reasonable interpretation of the term "characterizing", the Examiner submits that Pannell's "Addr Reg" sufficiently "characterizes" the entire block of 65,536 registers. While the Addr Reg may not "characterize" each of the 65,536 registers all at the same exact time, the Addr Reg is nonetheless capable of "characterizing" each of the 65,536 registers, just at different points in time during operation.

Additionally, the Examiner notes that the term “for” renders the limitation “selectively characterizing at least one of such blocks of registers as an indicated block of registers, such that any of the registers of the indicated block of registers may be addressed without adjusting a pointer” as merely a recitation of intended use of the claimed first register. A recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See MPEP 2111.04. With regard to the instant application, Pannell’s Addr Reg is at least capable of selectively characterizing at least one of such blocks of registers as an indicated block of registers, such that any of the registers of the indicated block of registers may be addressed without adjusting a pointer. Based on the foregoing, Pannell sufficiently discloses designating a first register within the plurality of registers that is separate from the blocks of registers for selectively characterizing at least one of such blocks of registers as an indicated block of registers, such that any of the registers of the indicated block of registers may be addressed without adjusting a pointer. Accordingly, the combination of Pannell/Law/Parlante renders claim 26 unpatentable.

36. With respect to Applicant’s argument regarding the first and second registers’ compatibility with IEEE standard 802.3 Clause 22, which appears on page 10 of the communication filed December 29, 2008, the Examiner respectfully disagrees. As is evident from pages 5-6 of Pannell, the two Clause 22 registers (Register 13 and Register 14) used in Pannell’s implementation are unused registers. (emphasis added)

Thus, it follows that not only are Registers 13 and 14 compatible with IEEE standard 802.3 Clause 22, but those two registers are also designated by the standard as available for vendor specification because they have been left unused by Clause 22. Based on the foregoing, Pannell sufficiently discloses both the first register and the second register being compatible with IEEE standard 802.3 clause 22 and designated by the standard as available for vendor specification. Accordingly, the combination of Pannell/Law/Parlante renders claim 26 unpatentable.

37. With respect to Applicant's argument regarding claims 30 and 31, which appears on page 11 of the communication filed December 29, 2008, the Examiner respectfully disagrees. For at least the reasons detailed directly above regarding claim 26, Pannell renders claims 30 and 31 unpatentable.

38. As for Applicant's arguments with respect to the dependent claims, the arguments rely on the allegation that the independent claims are patentable and therefore for the same reasons the dependent claims are patentable. However, as addressed above, the independent claims are not patentable, thus, Applicant's arguments with respect to the dependent claims are not persuasive.

Conclusion

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by MPEP 707.70(i):

CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, **claims 2-6, 8-13, 16, 18, 20-22, and 25-35** have received an action on the merits and are subject of a final action.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571) 272-1077. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2185

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Arpan Savla/
Examiner, Art Unit 2185
April 13, 2009

/Sanjiv Shah/
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